3D Packaging- Synthetic Quartz Substrate and Interposers for High Frequency Applications

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Abstract— Mobile communications and demands for instant data drive the need for smaller form factors with high performance and long battery life. Superior RF (Radio Frequency) substrates and 3D packages allowing the integration of higher bandwidth data into the mobile device have long been desired for accomplishing this goal. This paper introduces a new low-loss substrate that can be used as a standalone platform for RF design as well as a system for next generation 3D packaging for die-to-die interconnect. The next generation of mobile communication devices will operate at much higher frequencies to allow video on demand and video vis a vis RF communication. However, as frequencies rise, the need to reduce interconnects and integrate IC's continue to be in demand. Advanced packaging materials and processes will need to be developed, validated and implemented.

INTRODUCTION

Higher frequency designs now being implemented by electrical engineers are approaching millimeter wave lengths which impose interesting challenges for high volume standard substrates. Engineers have been able to work around certain problems but they are demanding new technology solutions as the next generation of devices are being introduced to the marketplace. These devices operate at >3GHz, transferring data >40 gigabytes/sec and server farms approaching Tera bits/second. This paper introduces a new set of substrates and technologies that are here to exceed the requirements of electrical and mechanical performance as well as being low cost.

Developing a substrate and packaging technology that is low cost, highly reliable, and available in high volume manufacturing and has design rules that enable the electrical engineer to design and simulate is not a trivial task. The complexity stems from the number of design elements that need to be satisfied. 1) Stable and predictable Dielectric Constant (Er) and Loss Tangent from 2-40 GHz, 2) Low cost metallization with high conductivity, 3) design rules and multiple manufacturing vendors that can fabricate designs into high volume products, 4) Substrates not effected by moisture and Er (Dielectric Constant) that are independent of temperature and frequency up to 50GHz, and, finally, 5) the substrate of choice must be available in a wide variety of thicknesses and sizes. In addition, the substrate must be compatible with current manufacturing equipment to allow easy adoption by the manufacturer.

Standard PWB laminates have enjoyed an almost overwhelming spectrum of new designs largely because engineers have been able to overcome high board losses. One of the reasons is that they are using advanced techniques for patterning and plating over thick Cu on the PWB. The challenge that is disruptive to this low cost board solution is being driven by high I/O count digital IC's with very high clock speeds. The PWB fabrication cost and complexity, however, is being driven higher by this dynamic and, as a result, manufacturers resort to combining board materials that are suitable for microvias, which also demonstrate good losses for RF design (i.e. Panasonic Megtron 6). What was once a $300 board is now greater than $15,000 per board. This results in combining packaging design and PWB board design which has many challenges. This paper offers a new solution to these challenges. We will describe the available substrates for high frequency applications, metallization, and the testing of those substrates at high frequency. The results of this testing then will be compared and contrasted for suitability at high frequency.

TECHNICAL APPROACH

Board/Packaging Material

As board design and packaging design techniques and methods converge, designers are looking for a middle ground where technology can offer benefits of both. Ceramic technology has been a solid performer and a good compromise in this area. However, recent demands of large WLP (wafer level packaging), where flatness across wafers the size of 200-300mm in diameter is essential, has become too stringent for ceramic and PWB technologies. This is where glass/quartz is far superior and, combined with low loss characteristics, offers the designer capabilities never before been realized until now. PCB materials and techniques are another solution. But as mentioned previously, these traditional solutions are cost prohibitive when the feature sizes of vias and traces are <4mils. Figure 1 lists a table of traditional materials used for packaging, board design, and WLP.

Substrate	**Dielectric Constant @18 GHz**	**Loss Tangent (10^{-4}) @18 GHz**	**Surface Roughness (Angstroms)**
Alumina	9.8	7	500
Synthetic Quartz	3.8	<1	10
Glass Sodium Free	5.9	30	300-1000
Soda Lime Glass	6.72	170	300-1000
Silicon	11.7 -12.7	150	2500
PCB(ceramic/Teflon)	2.94	14	3000
Sapphire	11.5	<1	10-100

Figure 1. RF Characteristics of Typical Materials

Typical substrate materials used for circuit design have printed wiring board (PWB) with copper foil, Alumina fired with tungsten and plated up with silver or gold, and a hybrid combination of hydrocarbon polymer and ceramic.

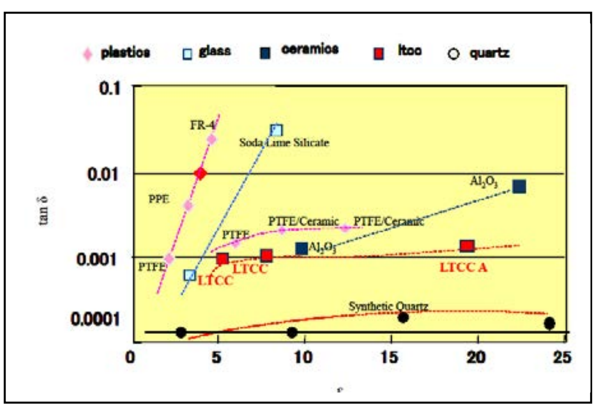

Figure 2. Loss tangent data for board/package materials.

The dielectric losses of these materials can be seen in the graph in Figure 2. These materials have been the choice of substrate materials for the past 50 years. Advances in electronics, design, form, and function have pushed the standard materials to the limit. Figure 2 shows the typical materials used in typical designs. However, as frequency increases, new materials need to be tested and qualified for high production use. Ceramic and glass materials have the lowest insertion loss. They have an added advantage of being hermetically and thermally stable throughout a wide variation of temperatures. Several types of alumina exist from standard Alumina to a form of Alumina called “Superstrate.” Synthetic quartz from AGC called AQ has low dielectric loss and has no piezo electric response usually associated with natural quartz (i.e. has the same losses in all directions)

Several types of glass exist on the market today but the glass that is sodium-free has the best frequency response. The reason lies with the electro negativity of the electron cloud loosely held by the sodium ion. During signal propagation, the electron cloud is distorted and results in the absorption of the energy, thus attenuating the signal. In sodium-free glass there is very little perturbation.

Surface smoothness is typically overlooked in high frequency applications. Surface roughness impacts signal integrity as a phenomenon known as skin effect [1]. As the frequency rises the signal predominantly propagates near the surface of the metallization resulting in an intrinsic rise in resistance. At frequencies greater than 30 GHz, the skin effect can be as high as 30% as shown in studies by Chai [2], et al.

Design Parameters

Figures 3 and 4 call out the design features that are currently achievable on glass and quartz. New developments are ongoing to achieve smaller diameter vias with tighter pitches in thinner and thicker glass and quartz for unique applications.

Parameter	**0.3mm thick Glass**	**0.25mm thick Quartz**
Via Diameter (d) (um)	50	50
Via Pitch (p) (um)	130	90
Via Conductors	Ag or Cu (not plated)	Ag or Cu (not plated)
Via Capture Pad (cp) (um)	d + 20	d + 20
Trace Width (w) (um)	10	10
Trace Gap (g) (um)	20	20
Trace Conductors	Cu or Ni/Cr/Au	Cu or Ni/Cr/Au

Figure 3. Design Parameters

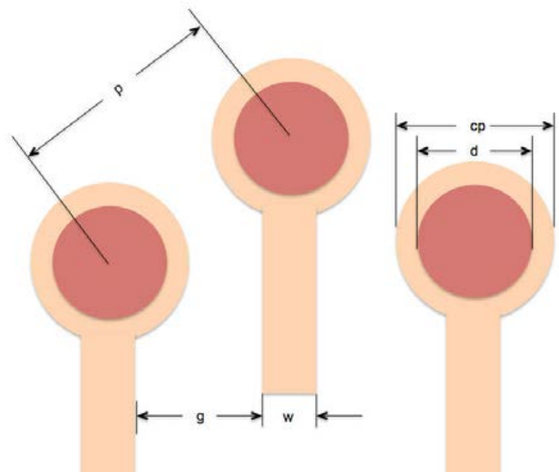

Figure 4. Design parameters for traces and vias

APPLICATIONS

3D Packaging

Adoption of high performance glass interposers are being driven by the need of electronics manufacturers where interconnects continue to shrink and battery life and heat are major concerns. Typical applications, such as computers, servers, graphic chips, and optical electronic moems are the main driving force. Because of the 3D nature of silicon and the need for precise placement and alignment, Glass/Quartz provides the most thermally stable substrate. In addition, advancements made in metallization (such as copper), fine-line width/spacing have now made these applications achievable at low cost while not compromising reliability.

Figure 5. TGV (Thru-Glass Via) Interposer

There are many ongoing industry efforts to support TSV (Thru-Silicon Vias) for interposers. This seems to be a logical fit since TSV's are being used on the wafer for routing the interconnect to the bottom of the die instead of traditional wire bond pads. The issues that we take with this approach are several, including, 1.) reliability is compromised at the PWB attachment point, 2.) the cost is higher due to the fact that they are processed in a Silicon Foundry clean room when fabricating the vias for the Interposers, and 3.) the Cu plating to create the Silicon vias has a significant mismatch to the PWB when soldered or epoxied. This causes cracking along the side walls which, in turn, entraps liquids from subsequent processes and later burns out during the thermal cycle of component attachment. These issues are typically not detected at the device level but further down stream at the component assembler or OEM (Original Equipment Manufacturer). Yield losses become progressively more expensive as the component moves downstream. Glass is a natural fit to resolve all of these issues when combined with a hermetically sealed via and used as a separator between the PWB and the Silicon IC.

RF Components

Synthetic Quartz, with its extremely low loss and low coefficient of thermal expansion, provides the ideal 3-D interposer for the RF designer who requires both high frequency performance and a stable substrate. Synthetic quartz with a surface roughness approaching single digit angstrom levels essentially negates skin effects in the millimeter wave range of use. Figures 6 and 7 show a component designed and fabricated on low loss synthetic quartz. The backside has solid metalization while the top side shows the design patterns with ground vias. There is a shadow that can be observed under the circuit traces which is due to the angle of the camera, lighting, and the high transparency quality of the synthetic quartz.

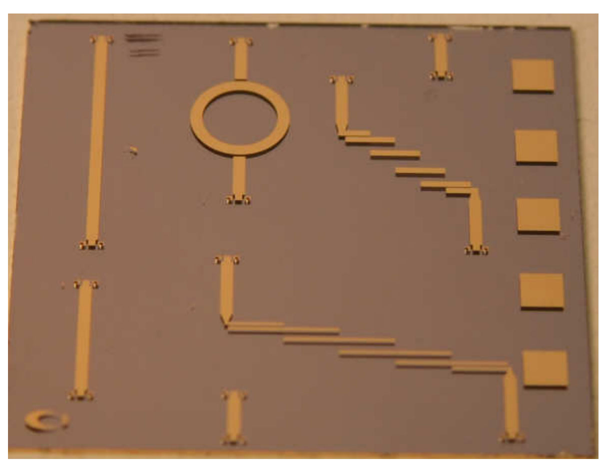

Figure 6 AQ1 Fabrication Coupon of RF Components

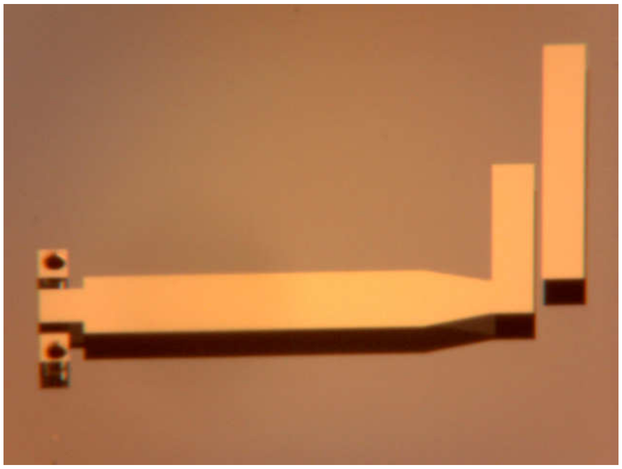

Figure 7. RF Feed line showing the ground vias

Figures 8 and 9 show the simulation results from Sonnet for both an 18GHz and 36GHz edge coupled filter. The combination of the low Er (i.e. wide traces), low surface roughness, low dielectric loss, and fine line widths/gaps, provides the designer an opportunity to design RF components with superior performance at low cost.

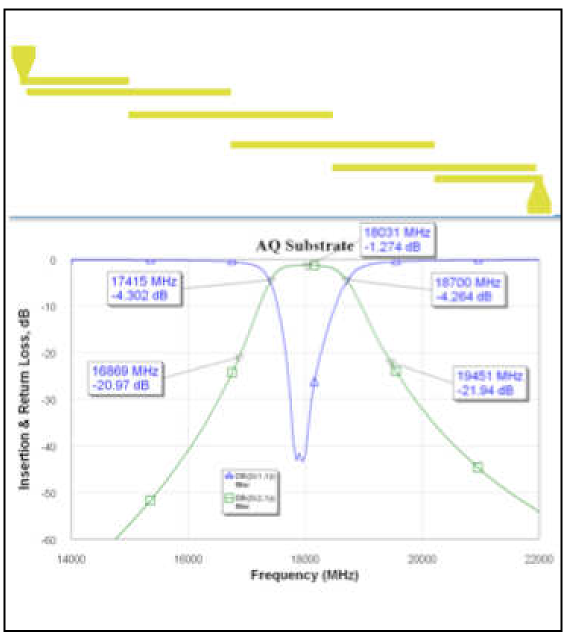

Figure 8. 18GHz Filter design on AQ1

The designs were implemented on 10mil thick AQ1 (low loss synthetic quartz) and 10 mil thick Alumina Superstrate from Coorstek. The measurement results in Figure 9 show that the AQ1 is quite superior to the Alumina Superstrate.

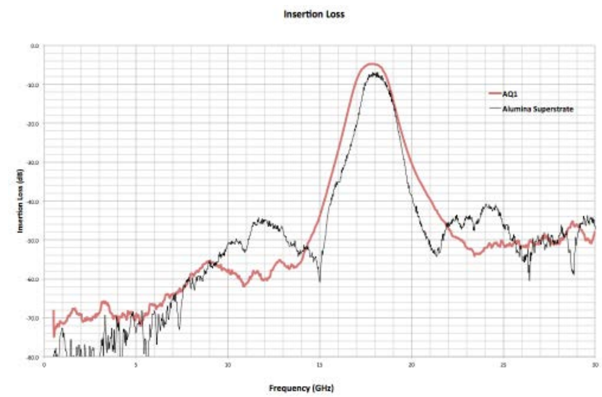

Figure 9. Measurement results of the 18GHz filter for AQ1 and Alumina Superstrate

The combination of lower dielectric constant (i.e. wider lines) and superior loss tangent gives the AQ1 a significant advantage over Alumina as well as the PTFE based materials (i.e. Rogers 6002). Figure 9 shows a 3-4dB improvement over Alumina, which is significant at 18GHz, when combining with amplifiers and other active signal processing IC's. The differences between the model and the measured are primarily attributed to the via connections to ground, as they were not included in the Sonnet model.

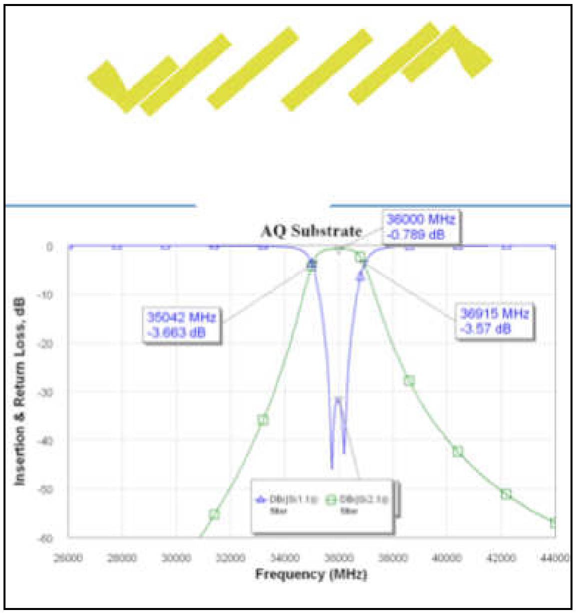

Figure 10. 36GHz Filter design on AQ1

RF Board Design

Glass/Quartz Interposers allow the ability to batch process utilizing LCD glass technology such as G4.5 (730 mm by 920 mm). Because of the stability of glass/quartz, scaling up of circuit design is feasible allowing designer to employ and leverage extremely large scale with flatness and roughness levels, unheard of for PWB and Ceramic board materials. Layout of circuit designs and rendering into precise substrates utilizing techniques developed in LCD technology drives cost down, and enables the designer to utilize the transparency of the glass in methods involved integration of electrical circuits, thereby eliminating interfaces and cost.

CONCLUSIONS

A new platform of packaging and board materials is upon us. This paper demonstrated designs that were achieved as 3D packages that we are calling TGV's. They are superior to Silicon TSV's and, as RF components, superior to the traditional board materials such as Alumina Superstrate. These new glass and quartz material platforms provide the designer with a low cost solution while providing hermetic, highly reliable packages and boards. Why sacrifice the reliability, as TSV's do, when glass and quartz materials are hermetic and can be used at lower cost?

Further work planned requires characterizing TGV's, and multi-layer RDL (Redistribution Layers) and surface roughness effects at 40-100 GHz. Thermal cycling and hermeticity testing of vias to demonstrate the robustness of the TGV system are currently underway.

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