Through Glass Via (TGV) Solutions for Wafer and Chip level Interposers and RF Integration Methods for High Frequency Applications

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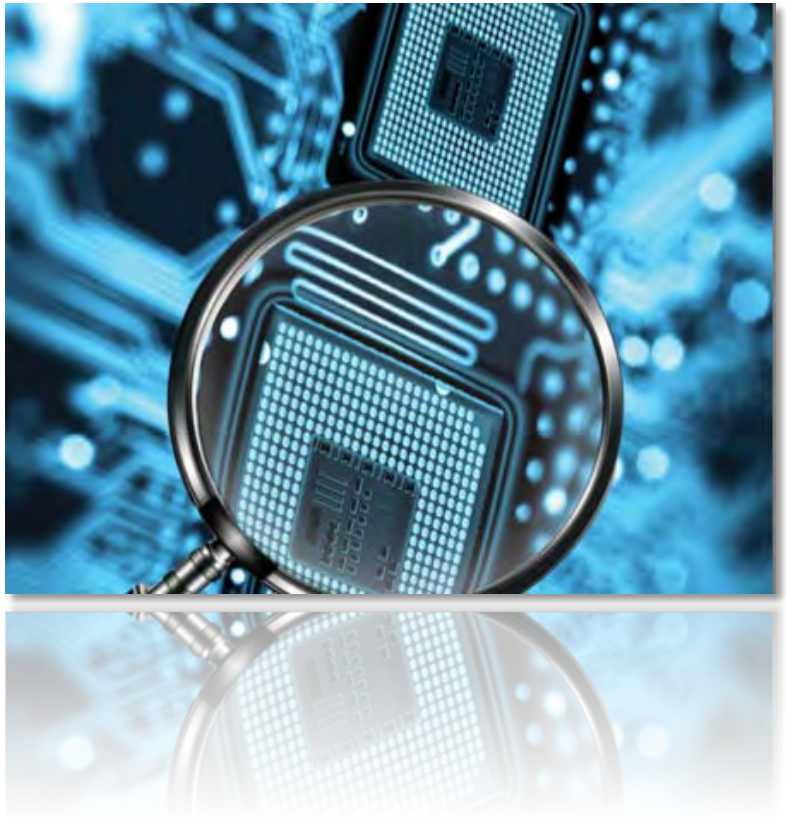
Emerging Industry

…focused primarily on overcoming the rapidly approaching barrier of the fundamental limits of silicon due to the phenomenal progress in current electronics and computer chip….(Moore's Law)

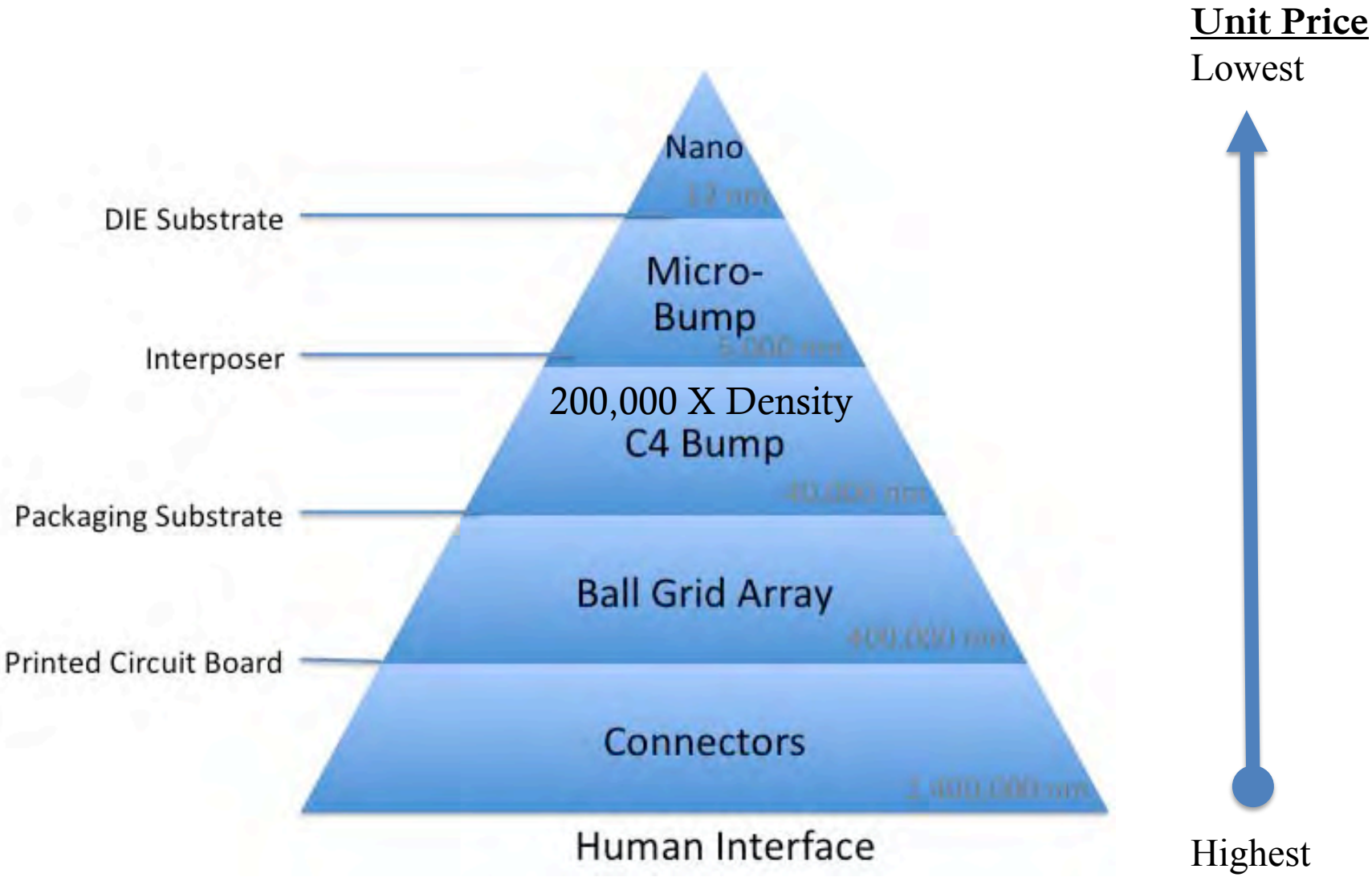


…including non-silicon based materials technologies to achieve low-cost, reliable, fast, and secure computing, communication, and storage systems.

DARPA

How to make the interconnect from the IC to the Outside World

Interface Pyramid



Electronic Density of 200,000 X

Why is Density & Interfaces Important?

- Integration at the top of pyramid leads to lowest unit price
- Cycle time for lowest unit price is the longest
- Interfaces drive cost because:
  - Unique tooling
  - Technical expertise
  - Test & manufacturing equipment
- Higher density chips are being introduced into the market for memory, processors, and wireless
- Presently, solutions at Printed Circuit Board level occupy the most real estate

Solution

Interface reduction ➔ Leads to faster cycle time & size reduction

Hermetic package ➔ Improves quality over time

Integrated solution ➔ Leads to lowest unit price

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DEFINITIONS

TGV
THRU-GLASS VIA

- Rigid Glass
- Bonded to Si Wafer
- Processed as a Wafer
- Softening 800-900°C
- Hermetic
- Non-RF
- CTE range 3.5 – 10 ppm/°C

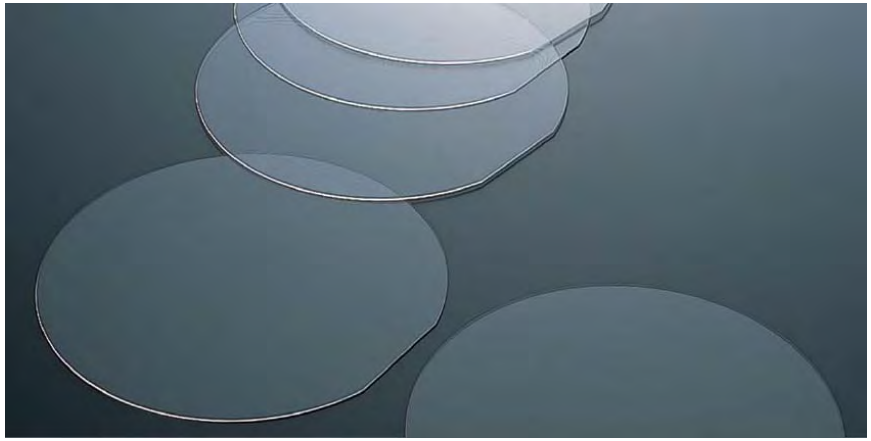
TQV
THRU-QUARTZ VIA

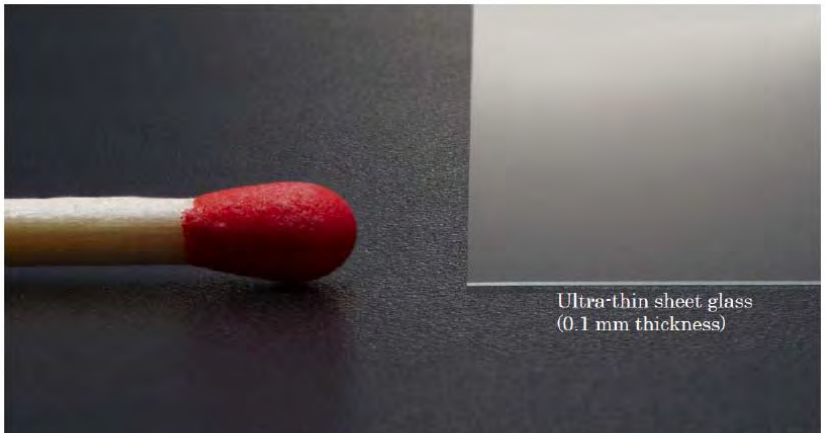
- Rigid Synthetic Quartz
- Die Attach
- Processed as a Panel
- Softening 1400-1600°C
- Hermetic
- High Frequency App's
- CTE range 0.5 – 1.0 ppm/°C

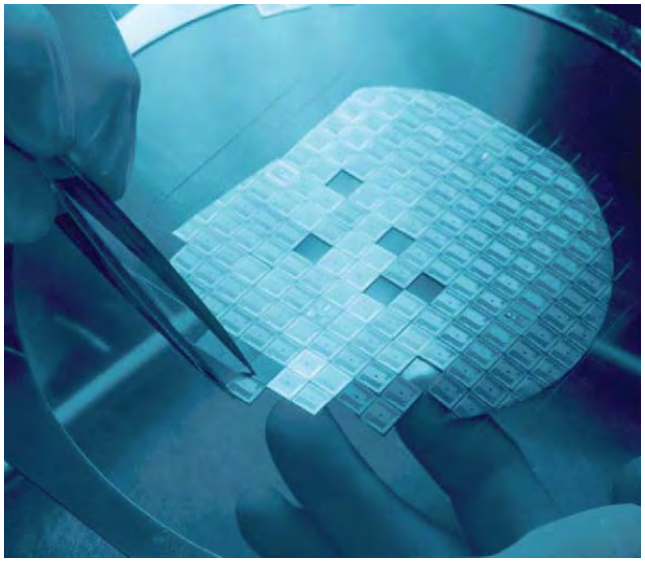
TFV
THRU-FLEX VIA

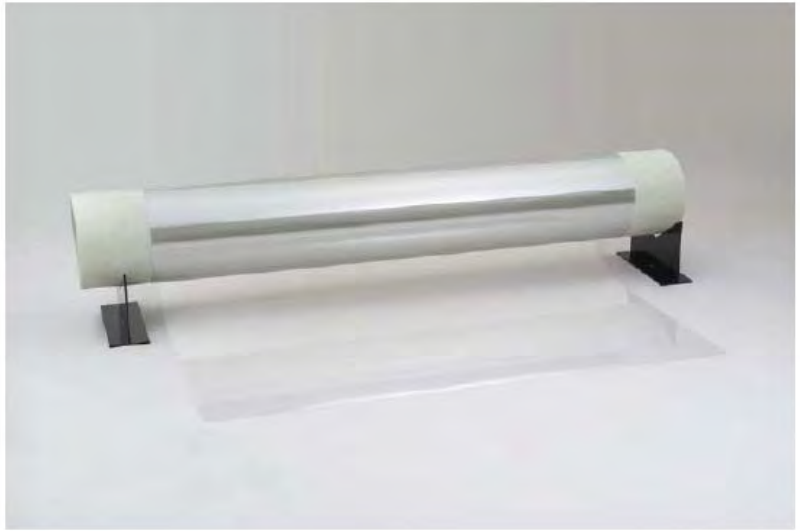
- Flexible Glass
- Softening 500-800°C
- Hermetic

Materials









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Materials

	Property	*Units*	*AQ*	*EN-A1*
Mechanical	Youngs Module	Ppa	74	77
	Knoop Hardness	GPa	6.4	
	Flexural Strength	Gpa	>100	
Electrical	Dilectric Constant	2-40 Ghz	3.8	5.8
	Insertiton Loss	2-40 Ghz	0.0002	0.02
Thermal	Bulk Resistance	Log (Ω-cm)	12.5	13.6
	CTE	ppm/°C	0.6	3.3
	Ts	°C	1600	950
	Tg	°C	1150-1200	720
Surface	Surface Roughness	nm	5	5
	TTV	um	<10	<10

AGC

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nMode TGV/TQV INTERPOSER PROCESS FLOW

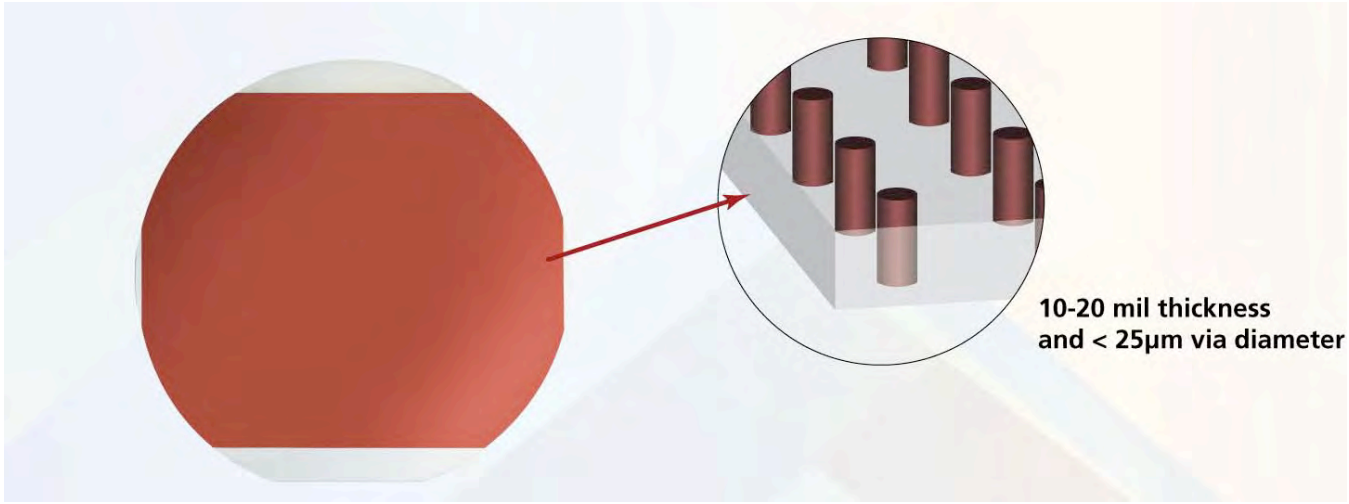
Material
- Substrate/Wafer Selection based on Electrical Performance & Design rules
- Polish to Specified Thickness
- Deposit Anodic Bond Layer

Via
- Drill Vias
- Inspect

Via Fill
- Fill Vias with TCE match Cu
- Polish Vias to surface of Glass

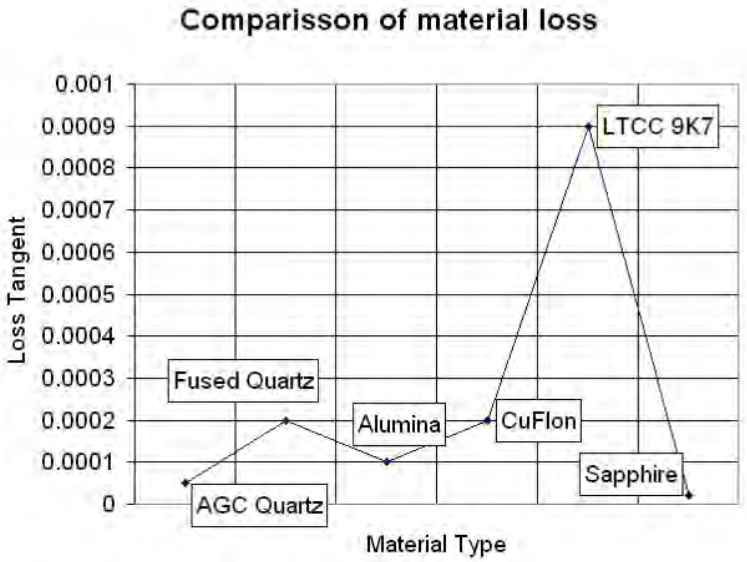
Circuit
- Add Cu (or standard Thin Film metals) to surfaces
- Pattern as required by the Design

Cu Interposer Technology



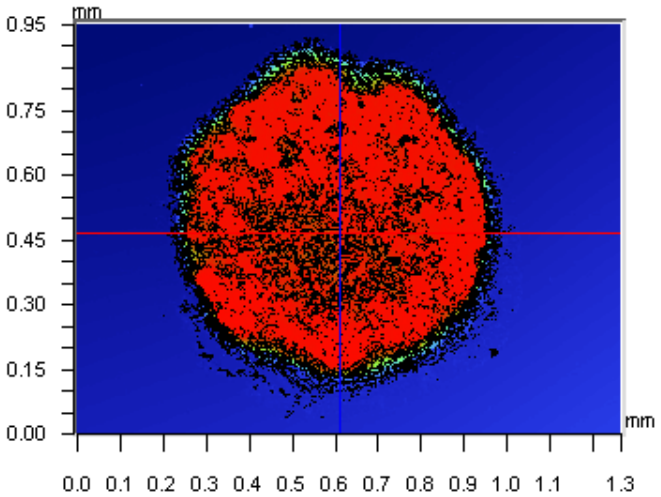
Key Merits:

- TCE Matched Cu to Substrate
- 25um diameter with 130um pitch
- Wafers or Substrates 250-500um thick,
- 200 or 300mm wafer diameter/size are typical
- Can be supplied with High Performance Synthetic Quartz or Glass
- Ideal for Use with TSV for WLP
- Hermetic
- RDL (Re-Distribution Layers) can be applied
- Via Conductivity: 1.6 - 1.9 mΩ/□ (4.5 X 10^7 S/m)

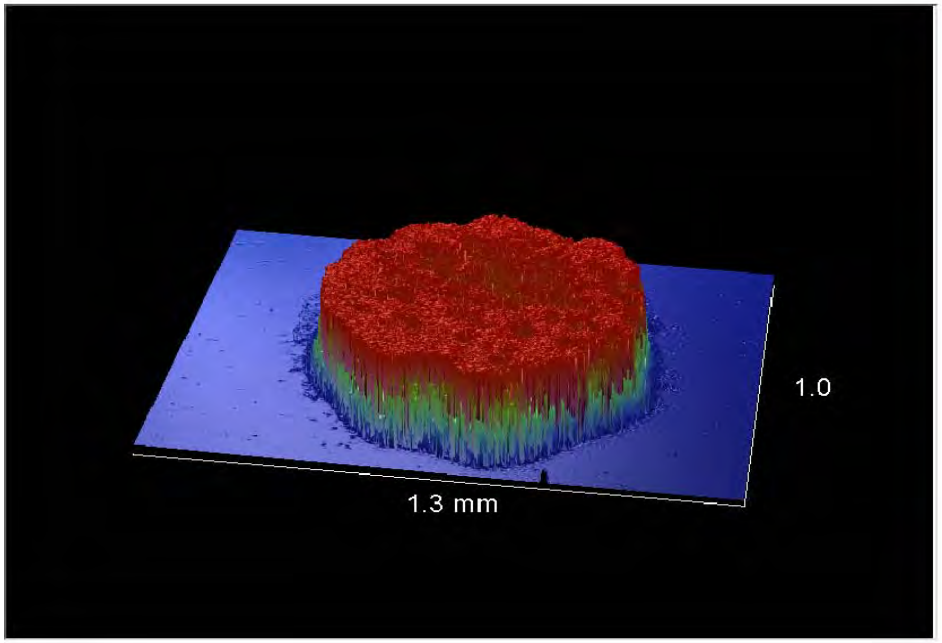


Lowest Loss Material / Circuit on the Market

Cu Via - TGV



Cu Density and Size



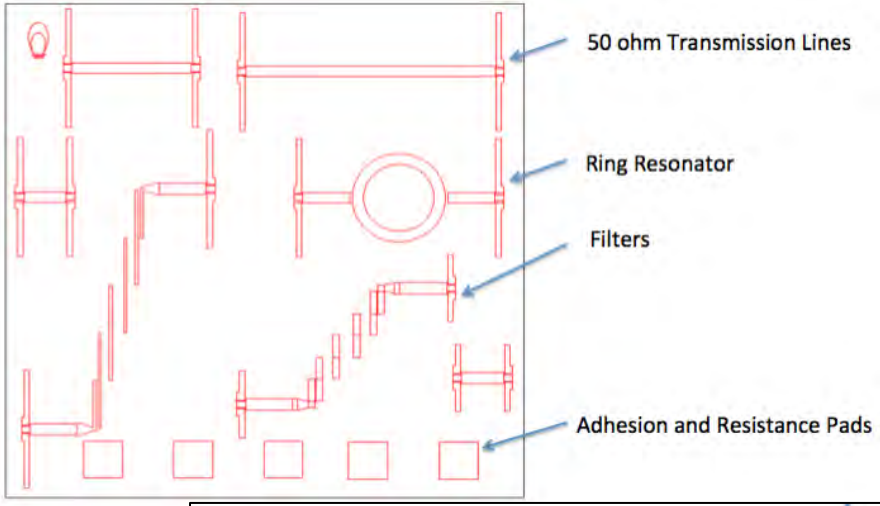
Profile of Via prior to "Kiss Polish"

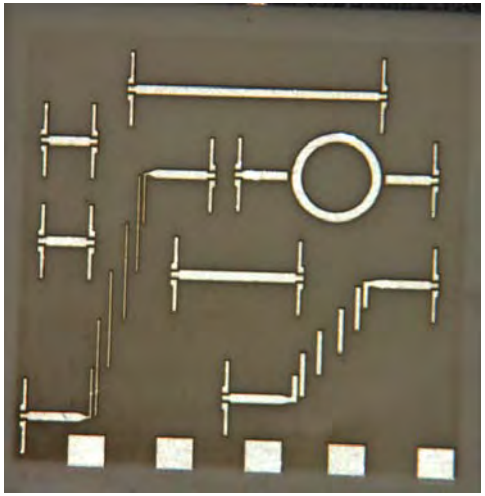
Surface Profile on EN-AQ post Via Processing

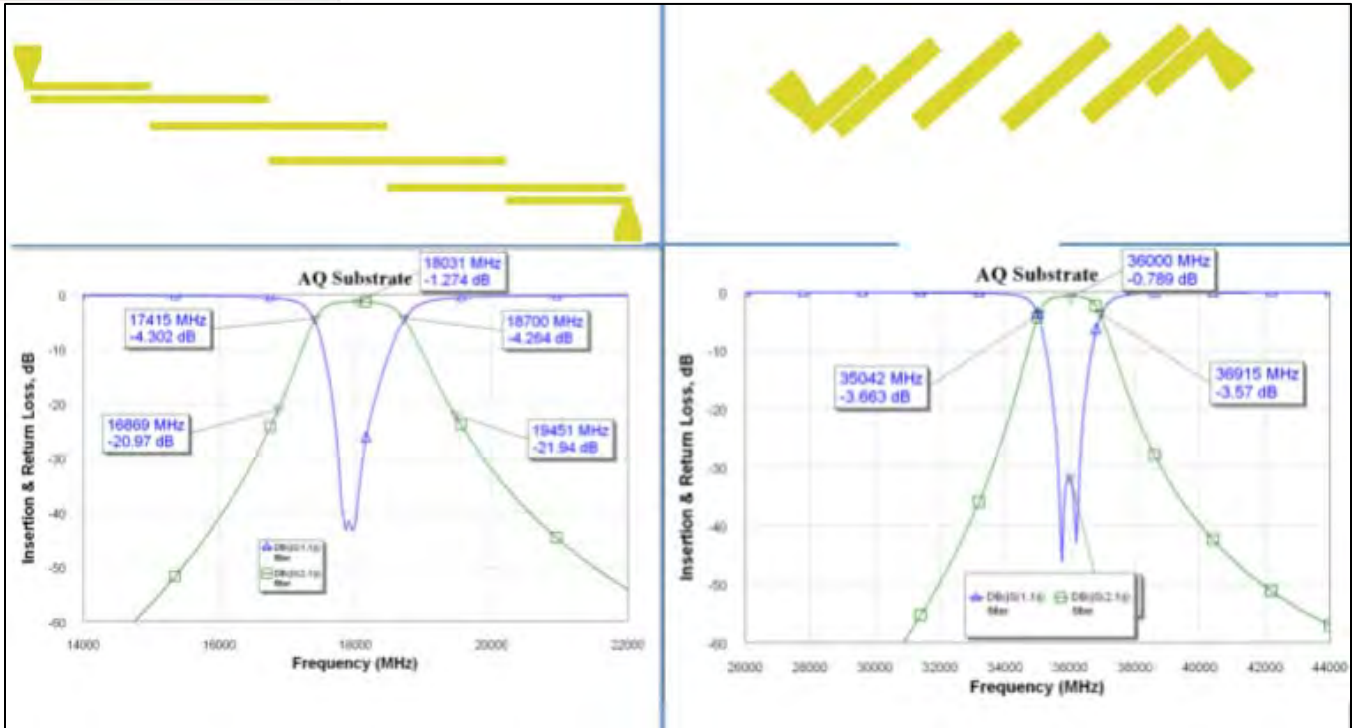
Rq	0.10	um
Ra	0.08	um
Rt	0.44	um
Rp	0.30	um
Rv	-0.14	um

Angle	29.72	urad
Curve	0.64	m
Terms	None	
Avg Ht	0.04	um
Area	52.22	um2

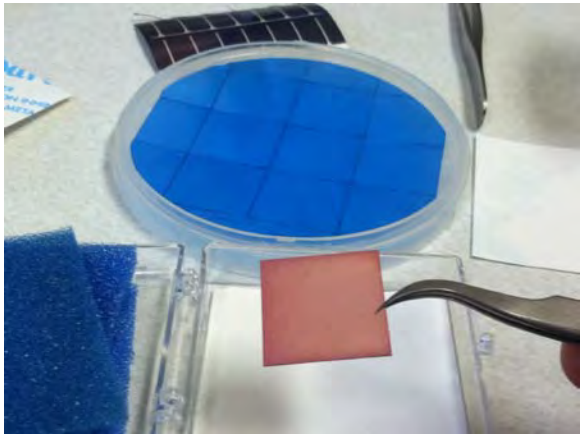
EMBEDDED RF COMPONENTS

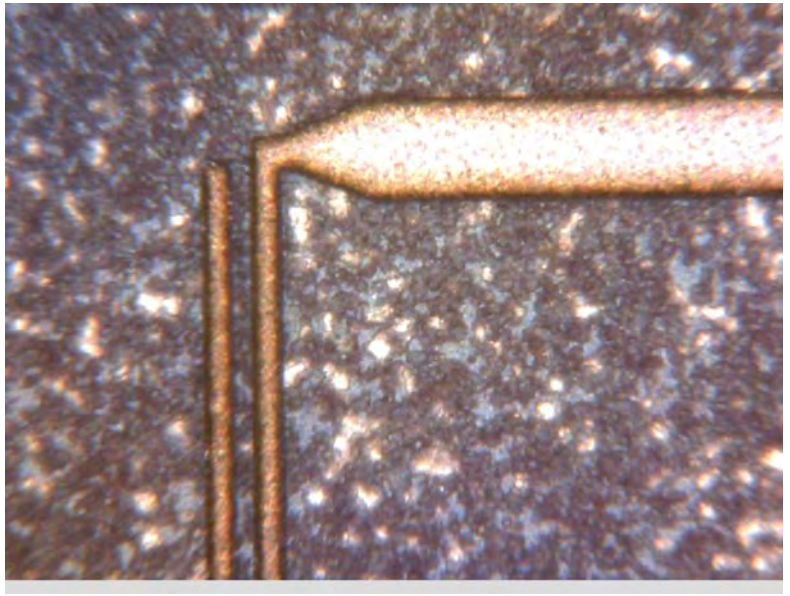


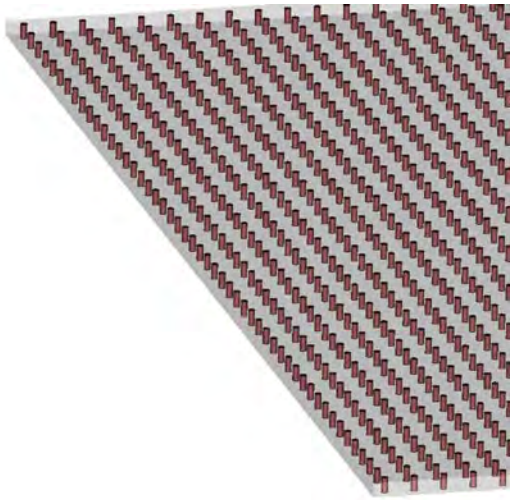




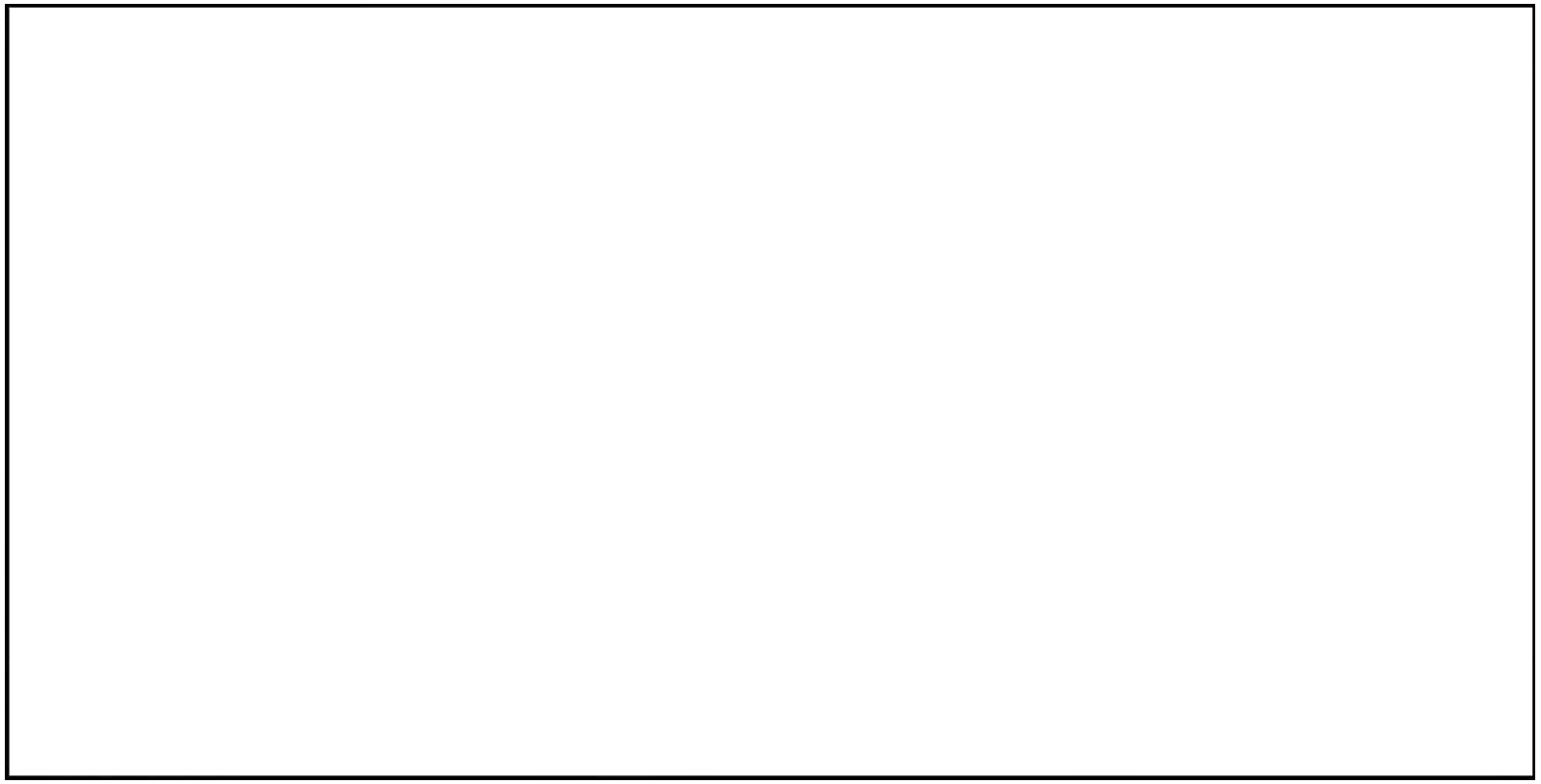
Substrates, Patterns, and Vias





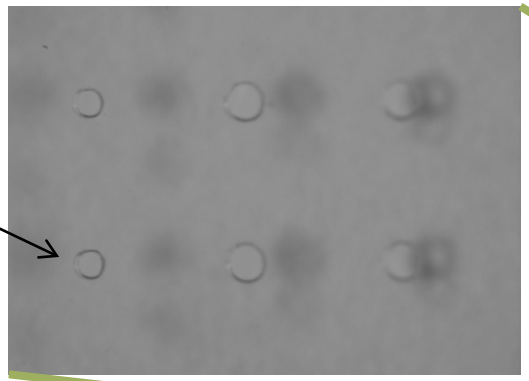


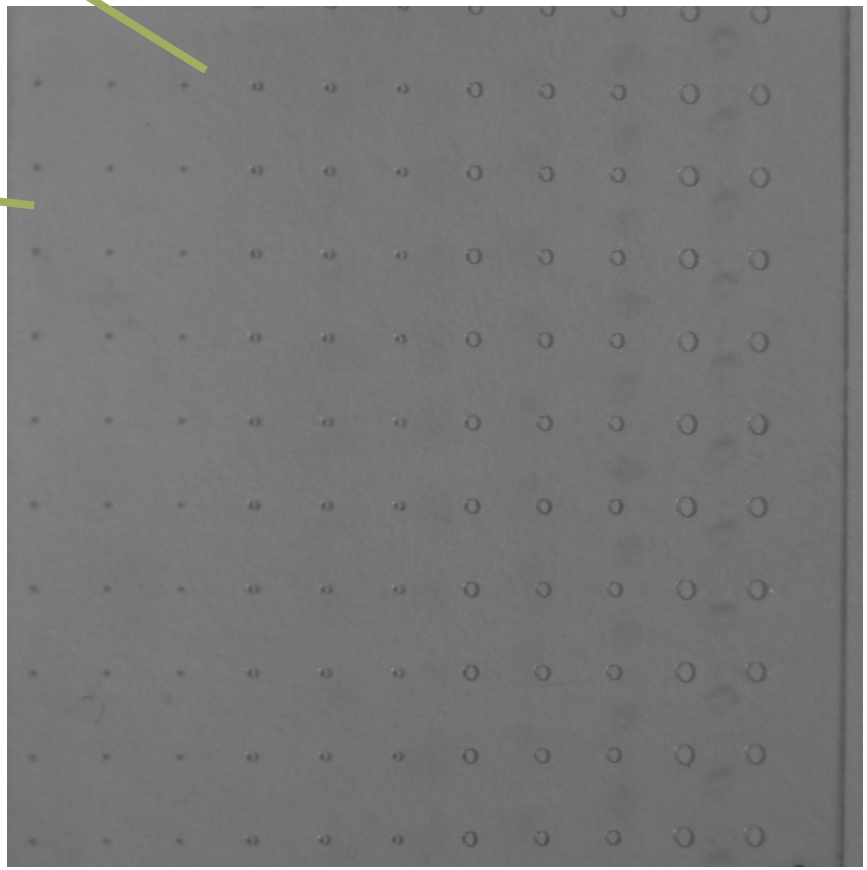
Interposer Performance



…Low loss like Sapphire
…Low cost like PTFE laminates

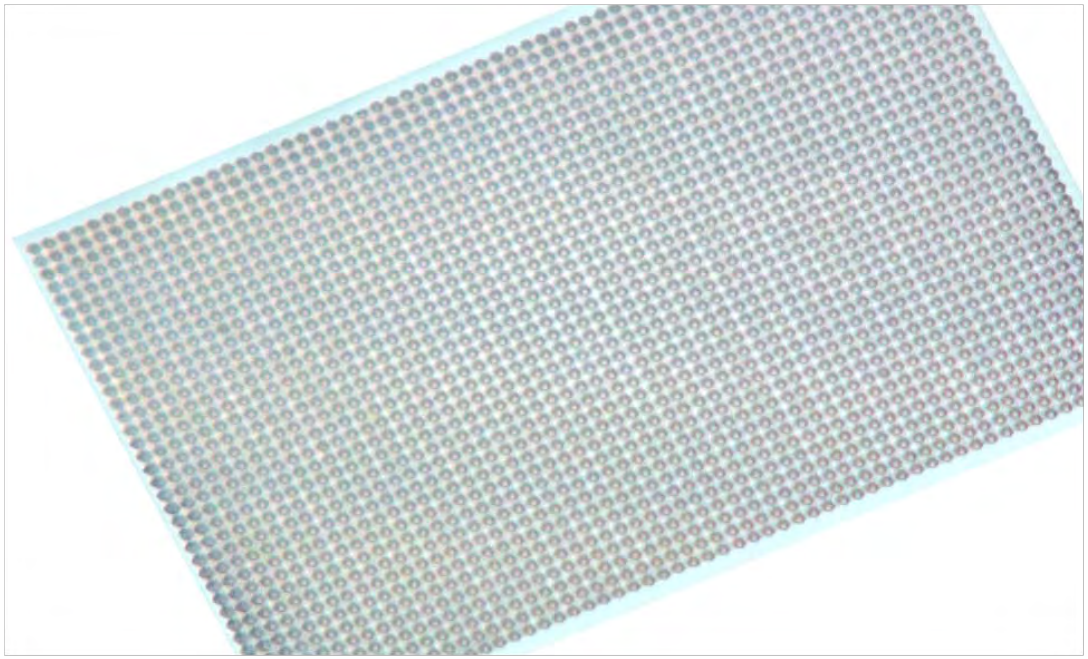
TGV - Non-Filled Via





250um thick substrate
Largest via is 15mils diameter
Smallest via is 2mils diameter
Exit and Entry side are within 1% of each other

TQV - Die Attach Interposer



- 50um Diameter Vias
- 130um Pitch
- 250um Thick Quartz Substrate
- 2,242 vias for this 5mm X 7.5mm part
- ~ 15 seconds / per part to drill vias
- Vias are Solid Filled Cu for a ***Hermetic*** via
- Cu is a Cu/Glass Composite, TCE matched to the glass, then polished

Interposer Substrate Technologies

		TGV	TFV	TQV
Demonstrated Efforts	Min Dia Via (um)	50	40	50
	Min Via Pitch (um)	130	R&D	130
	Min Substrate thickness (um)	300	30	250
	Min line width/space (dry etch)	25	R&D	25
Properties	Via Type	Cu or Ag	R&D	Cu or Ag
	Hermetic	check	R&D	check
	Primary Advantage	No Sodium	Thin and Flex	Lowest Loss on the Planet

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FINAL WORD

Post assembly on a PWB, part may experience:

- 20-40 thermal cycle events
- Board washing/rinsing in cleaning fluids
- Migration of solder away from the solder joint
- Debris contamination from nearby re-work

Which may cause circuit failure at the DIE level

Using glass between the DIE and PWB can prevent Failures

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